Process window enhancement using advanced RET techniques for 20nm contact layer

Yang Ping[a], Sarah McGowan[a], Ying Gong[b], Yee Mei Foong[b], Jian Liu[c], Jianhong Qiu[d], Vincent Shu[d], Bo Yan[d], Jun Ye[d], Pengcheng Li[d], Hui Zhou[d], Taksh Pandey[d], Jiao Liang[d], Chris Aquino[d], Stanislas Baron[d], Sanjay Kapasi[d]
a – GLOBALFOUNDRIES Inc., 2600 Great America Way, Santa Clara, CA 95054, USA
b – GLOBALFOUNDRIES Inc., 60 Woodlands Industrial Park D Street 2, Singapore 738406
c – GLOBALFOUNDRIES Inc., 400 Stone Break Road Extension, Malta, NY 12020
d - ASML Brion, 4211 Burton Dr. Santa Clara, CA 95054, USA

ABSTRACT

At the 20nm technology node, it is challenging for simple resolution enhancements techniques (RET) to achieve sufficient process margin due to significant coupling effects for dense features. Advanced computational lithography techniques including Source Mask Optimization (SMO), thick mask modeling (M3D), Model Based Sub Resolution Assist Features (MB-SRAF) and Process Window Solver (PW Solver) methods are now required in the mask correction processes to achieve optimal lithographic goals. An OPC solution must not only converge to a nominal condition with high fidelity, but also provide this fidelity over an acceptable process window condition. The solution must also be sufficiently robust to account for potential scanner or OPC model tuning. In many cases, it is observed that with even a small change in OPC parameters, the mask correction could have a big change, therefore making OPC optimization quite challenging. On top of this, different patterns may have significantly different optimum source maps and different optimum OPC solution paths. Consequently, the need for finding a globally optimal OPC solution becomes important.

In this work, we introduce a holistic solution including source and mask optimization (SMO), MB-SRAF, conventional OPC and Co-Optimization OPC, in which each technique plays a unique role in process window enhancement: SMO optimizes the source to find the best source solution for all critical patterns; Co-Optimization provides the optimized location and size of scattering bars and guides the optimized OPC solution; MB-SRAF and MB-OPC then utilizes all information from advanced solvers and performs a globally optimized production solution.

With this approach, we will demonstrate that, with a holistic RET solution, the process window can be significantly improved for 20nm contact layers.

Keywords: Optical Proximity Correction (OPC), Source Mask Optimization (SMO), Model Based Sub Resolution Assist Feature (MB-SRAF), low-k1 lithography

1. INTRODUCTION

As design rules shrink, and the lithography k1 value is pushed below 0.3, it is very hard to obtain acceptable process window and MEEF (Mask Error Enhancement Factor) because of the low image contrast and the complexity of the pattern shape. Besides techniques like litho-friendly design, double patterning, and image contrast improvement by means of negative-tone development (NTD), computational lithography remains the key enabler for process window enhancements for contact layers. Resolution enhancement techniques (RET) such as use of free-form pupils obtained by source and mask co-optimization (SMO) instead of parametric sources, use of model-based assist feature placements (MB-SRAF) as opposed to rule-based SRAF placements, use of advanced optical proximity correction (OPC) solvers like process window solver and Co-optimization solver are essential for achieving high-fidelity patterns and wide process window. In this study, we use such a holistic approach to attain the process window necessary for full-chip production runs.

Optical Microlithography XXVII, edited by Kafai Lai, Andreas Erdmann, Proc. of SPIE Vol. 9052, 90521N © 2014 SPIE · CCC code: 0277-786X/14/$18 · doi: 10.1117/12.2048513

This paper is organized as follows: Section 2 discusses process window enhancements obtained by using SMO compared to old illumination source. SMO is typically done using few carefully-chosen critical clips in order to achieve the required process window. To match the SMO performance on full-chip, various techniques and flows including SRAF optimization, process-window-aware OPC, SRAF print avoidance and co-optimization OPC are used, as described in Section 3. Verification and process window comparison between SMO simulation and full-chip OPC results are presented in Section 4.

2. SOURCE MASK OPTIMIZATION

2.1 Layout and pattern selection

The 20nm contact layer in question contains patterns with both square contacts and long rectangular contact shapes. Various designs of dense-pitch contacts, isolated contacts, line-end to line-end and critical SRAM patternswere included. The selected patterns also include rectangular contact patterns in both orientations, which is challenging for contact printing.

2.2 SMO flow

ASML Brion's Tachyon SMO^{TM} software was used for the optimization of the illumination source and the mask layout. The illumination source used in this work was a free-form source using ASML's FlexRay^{TM} programmable illuminator. An optimized full-chip SMO flow was used to optimize the illumination source for all the critical patterns, with reasonable simulation turnaround time [1].

The simulation was carried out for a clear-field mask with NTD processing. Defocus, dose variation and mask bias were key parameters for the source optimization, as well as OPC, within the SMO flow. Mask rule checking (MRC) was used as a constraint for co-optimization. The 3D Mask effect was considered in all simulations. Depth of focus (DOF), exposure latitude (EL) and mask error enhancement factor (MEEF) were used to evaluate the SMO simulation result.

Table 1. Process window comparison between old illumination source and the new SMO source.

	DOF @ 5% EL	MAX EL	MAX MEEF
New SMO source % Improvement	+59%	+24%	-16%

Simulation results were compared for the old illumination source and the new SMO source. A pixel-based OPC solution was used for both simulations, to achieve the optimum OPC results. DOF, EL and MEEF simulation results are illustrated in Table 1. It was shown that the new SMO illumination source provided improved process window with increased DOF and EL, as well as decreased MEEF. However, the SMO Mask-Optimization (MO) OPC solution (Figure 1) that provides this superior OPC simulation result may not be applied for full chip OPC due to runtime considerations. Therefore, it is necessary to verify the new SMO source with a full-chip compliant OPC solution, as discussed in the next section. The PVBAND shown in Figure 1 is generated by varying the focus, the exposure dose and the mask bias conditions.

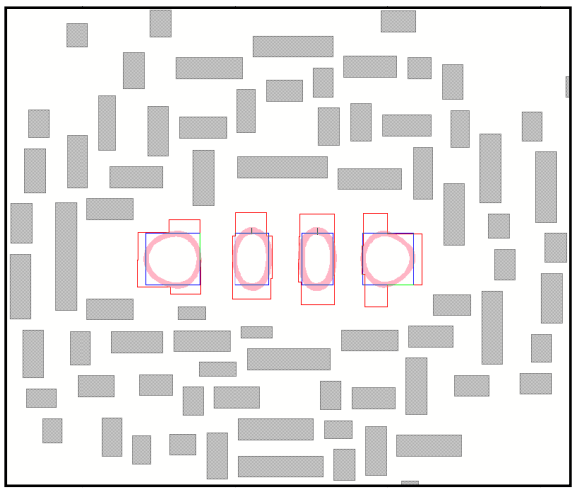


Figure 1. OPC example in SMO simulation showing PV bands.

3. FULL CHIP OPC OPTIMIZATION

After the new SMO source was generated, a new OPC model was calibrated. Mask 3D effects are included in the OPC model. The OPC optimization results discussed in the following sections were achieved based on this calibrated OPC model. Figure 2 depicts the baseline OPC flow that is described in this paper.

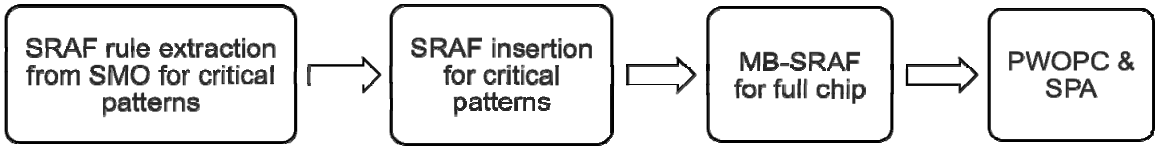
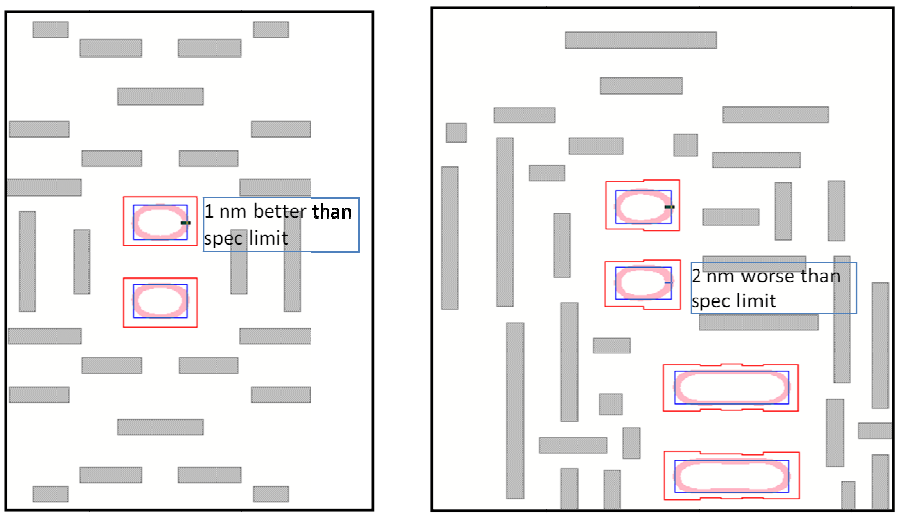


Figure 2. Baseline OPC flow using SRAFs and PWOPC.

3.1 SRAF placement optimization

The use of SRAFs has been widely adopted for process window improvement. With simple designs and regular pattern shapes, rule-based SRAFs (RB-SRAFs) can work well and are sufficient to provide the necessary process window margin. However, as the technology shrinks, design complexity as well as the adoption of pixelated illumination sources has made SRAF rule generation a very challenging and time-consuming task. In addition, RB-SRAF is heuristic-based, and one cannot guarantee that the SRAFs are placed at the optimal location for all the design patterns. Inadequate SRAF coverage on complex 2D patterns can happen due to incomplete sets of rules.

MB-SRAF solvers alternatively analyze the aerial image and place SRAFs automatically at optimum locations, while also taking mask proximity effects into account. Major OPC vendors in recent years have also reduced MB-SRAF generation runtime and transformed to use exclusively rectangular SRAF shapes, which makes MB-SRAF a full-chip-capable solution. However, other challenges still exist for MB-SRAF, including SRAF inconsistency issues, which can result in process variation on wafers. Since MB-SRAF uses OPC model simulation to determine the SRAF guidance map (SGM) for SRAF placement, a small change or perturbation in the proximity can result in SRAF placement differences and process variation band (PVBAND) differences. Figure 3 demonstrates two MB-SRAF placements with different environments in the design target. Due to the differences in the proximity and the SRAF placement, a 3 nm variation is noticed in the PVBAND after OPC is applied, which could lead to erroneous yield characterization analysis.



(a) (b)

Figure 3. Two different MB-SRAF placements cause a 3 nm variation in PVBAND. (a) MB-SRAF for isolated two-contact case; (b) MB-SRAF for two-contact case with other design pattern in the neighborhood.

MB-SRAF consistency issues have been greatly improved with the latest Tachyon OPC software from ASML Brion. SRAF consistency can be maintained within a user specified range for repeated target patterns, using Super Symmetry (SUSY) functionality. SUSY groups segments with identical environments, within a range, in the same category, thereby enforcing same SRAF placement for those segments. Figure 4 illustrates OPC mask variation for OPC runs with and without SUSY functionality. The histogram data is generated from more than 16,000 gauge locations on repeated design target patterns. It can be shown that using SUSY functionality for MB-SRAF can greatly improve the OPCed mask. The decrease in mask variation can also reduce the impact of mask processing error, which is a big impact on process variation. It can be noted that even when SUSY is enabled, certain mask variations still exist for a small group of segments. It is speculated that these variations arise from OPC discrepancies near the boundary between neighboring layout blocks. Further investigation will determine the root cause of these variations.

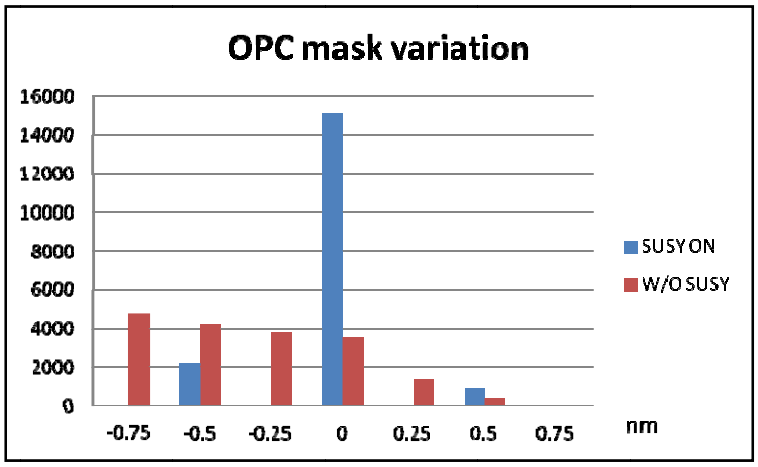
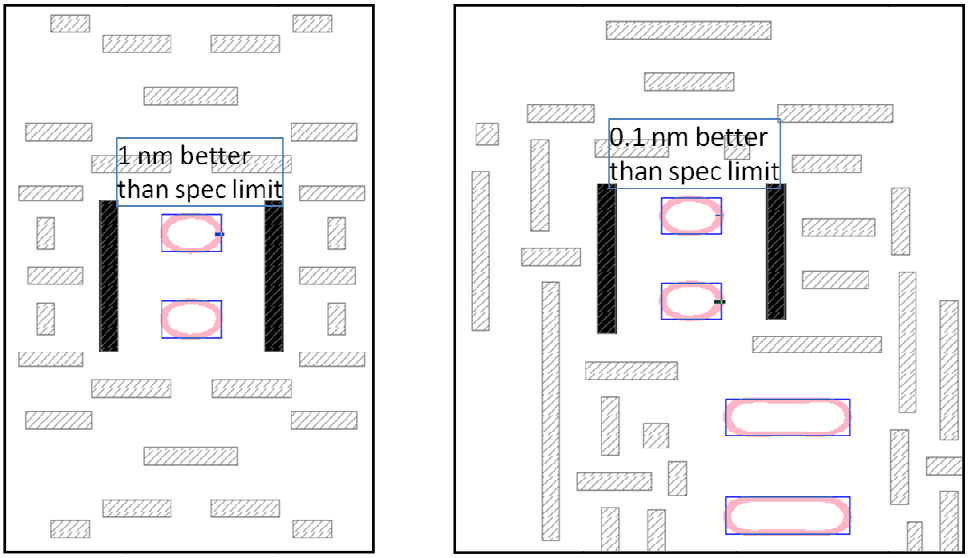


Figure 4. OPC mask variation or correction variation comparison with and without SUSY functionality

To further reduce the process variation for other critical design patterns without repeatability issues, we can insert SRAFs extracted from SMO for selected logic design patterns. The inserted SRAFs were subject to MRC clean-up during MB-SRAFs insertion to ensure the final OPC results are mask rule compliant.



(a) (b)

Figure 5. Hybrid SRAF solution for two similar design patterns. The solid SRAFs were inserted based on SMO approach and the rest of the dashed SRAFs were placed using pure model-based approach.

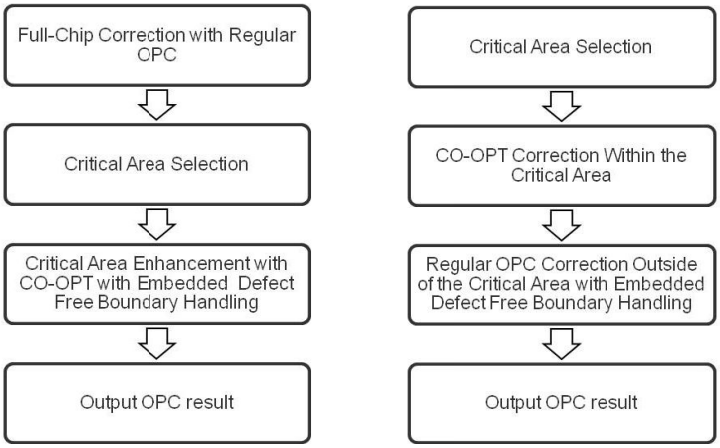
Figure 5 demonstrates this hybrid SRAF solution, where the solid SRAFs were placed first based on SMO approach for selective design target patterns only, and the cross hatched SRAFs were placed using pure model-based approach. The improvement of SRAF consistency with this approach reduces the process variation for the selected critical patterns, while MB-SRAFs provide the optimum solution for the rest of design patterns. The variation of simulated PVBAND is improved to 1 nm (Figure 5), compared to 3 nm variation as shown in Figure 3.

3.2 SRAF-MF co-optimization

Even with MB-SRAF and PWOPC, the OPC flow described in the above sections may not be enough to provide the necessary process window for certain critical patterns, especially in low contrast and high MEEF areas where the interaction between segments and the interaction between MFs and SRAFs are strong. Cost-based OPC solvers such as a Matrix OPC solver or multiple variable/segment OPC solver have been adopted in full-chip OPC to improve OPC convergence and to solve MRC-constrained OPC problems [2, 3, 4]. These cost-based OPC solvers generally take into account the interaction between multiple edge segments on the MF by solving a large Jacobian matrix problem in selected regions. However, the strong interaction between MFs and SRAFs now requires the OPC solver to correct both the MF segments and SRAF segments simultaneously to achieve the optimum OPC solution, like Inverse Lithography Technology (ILT) does, while the OPC runtime needs to be kept at a reasonable level. For example, an edge movement on the MF can cause a nearby SRAF from non-printing to printing. Similarly, SRAF shrinking or SRAF chopping during correction can cause process window degradation on nearby MFs.

The Co-optimization (CO-OPT) OPC tool from ASML Brion provides such SRAF-MF co-optimization capability by extending the multiple variable solver to correct a large amount of segments together including both the MFs and SRAFs. Such an OPC solver generally cannot be applied to the full chip due to its relatively slower runtime performance. However, the runtime is manageable when the CO-OPT OPC is only applied in selective hot spots.

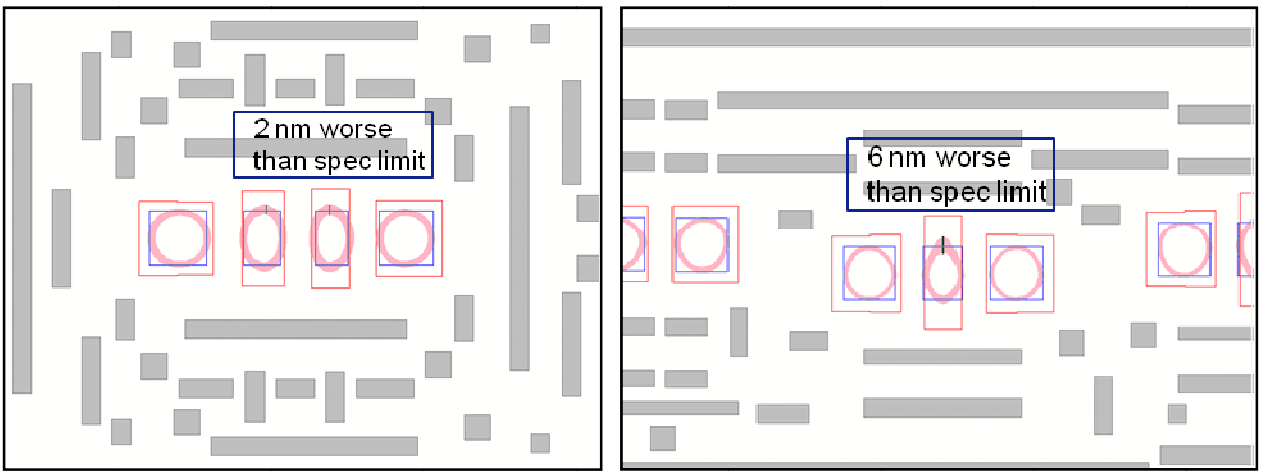
Figure 6 shows two possible OPC flows using CO-OPT OPC. For the work described in this paper, we have chosen flow (a) as the full chip solution, which can be described as a hybrid OPC solution.



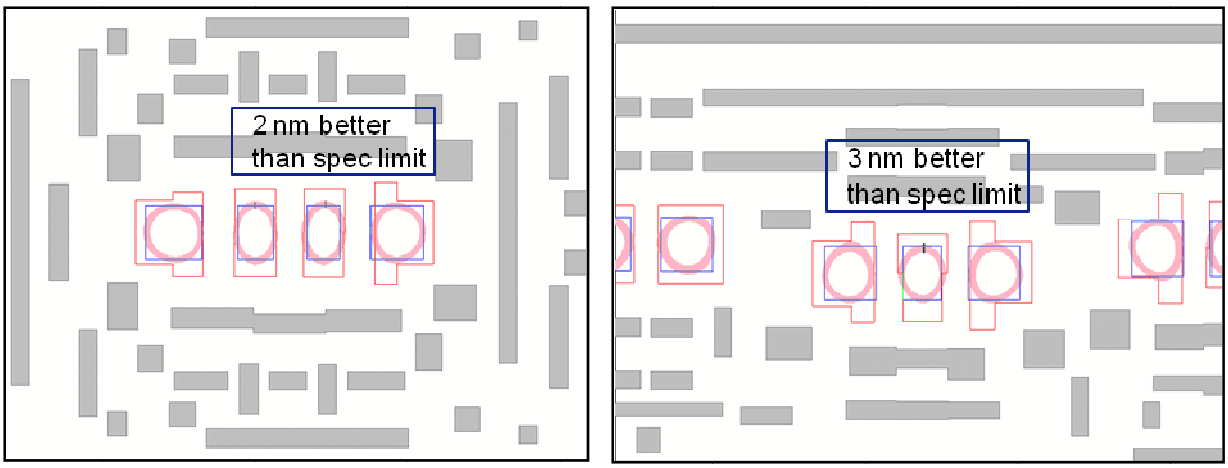
(a) (b)

Figure 6. Two OPC flows using CO-OPT OPC. (a) Regular OPC is applied for the full chip first followed by CO-OPT OPC on selected area; (b) CO-OPT OPC is applied to selected critical area first followed by regular OPC for the rest of the full chip.

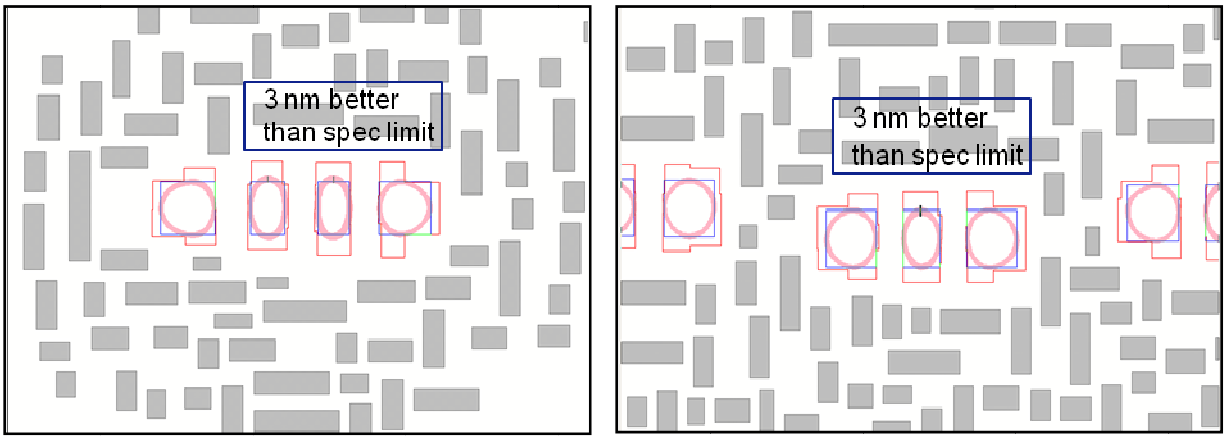
Figure 7 compares the simulated PVBAND for OPC results using regular OPC, the CO-OPT OPC and MO OPC. The simulation is performed on a four-contact case and a three-contact case, which are considered weak geometries with the given illumination source. Figure 7 (a) shows the regular OPC result and simulated PVBAND. The image contrast is low for this case, and the interactions between neighboring segment edges (including SRAFs) are strong. It is challenging to find the optimum OPC solution by solving the MFs alone. The worst PVBAND is measured at 6 nm worse than spec limit for the middle contact. By using CO-OPT OPC for this pattern, both MFs and SRAFs are co-optimized together, and the worst PVBAND is significantly improved to 2 nm better than spec limit, as illustrated in Figure 7 (b). In addition, the simulated PVBAND result from the CO-OPT OPC matches closely to what MO OPC provides as shown in Figure 7 (c), which is considered the optimum solution given the illumination source and mask type. The PVBAND is generated by varying the focus, the exposure delta dose and the mask bias conditions.



(a) OPC result with regular OPC. The worst PVBAND is 2 nm worse than spec limit for case 1 and 6 nm worse than spec limit for case 2.



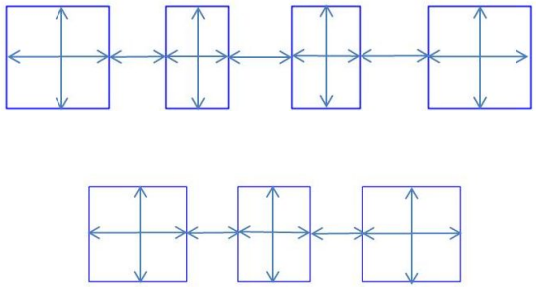
(b) OPC result with CO-OPT OPC. The worst PVBAND is 2 nm better than spec limit for case 1 and 3 nm better than spec limit for case 2.



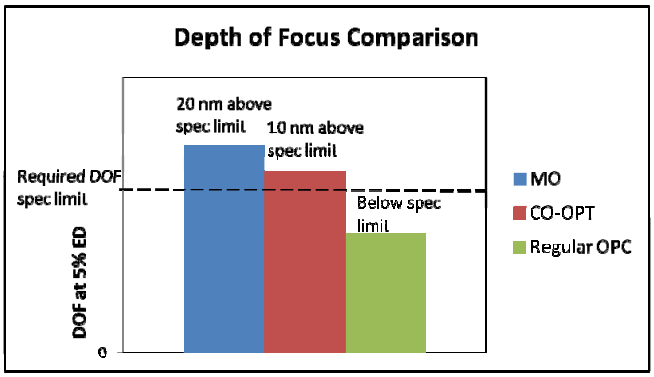
(c) OPC result with MO. The worst PVBAND is 3 nm better than spec limit for case 1 and 3 nm better than spec limit for case 2.

Figure 7. Simulated PVBAND results for regular OPC, CO-OPT OPC and MO.

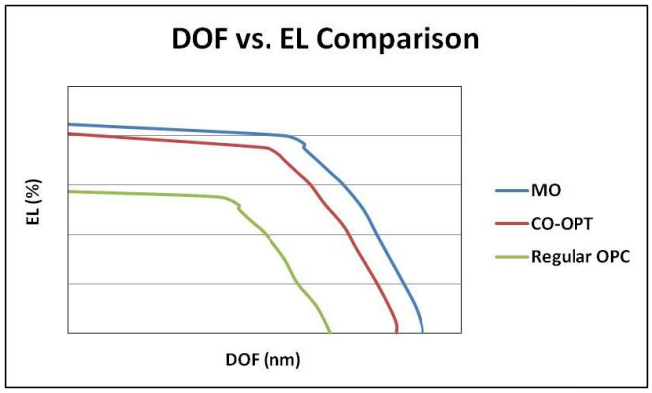
Figure 8 further compares the simulated process window in terms of DOF and EL for the three different OPC techniques: MO, CO-OPT and regular OPC. Both the four-contact case and the three-contact case are included in the characterization. Multiple cut lines including both contact width and space are used (Figure 8 (a)), and the simulations are performed based on overlapping process window among all the cut line locations, allowing ±10% CD or space variation. With regular OPC, the overlapping process window is very poor. By applying CO-OPT OPC after regular OPC, both DOF and EL are improved significantly. In addition, the simulated process window result from CO-OPT OPC matches closely to what MO provides. DOF for CO-OPT OPC exceeds the required DOF spec limit at 5% EL and is only 10 nm smaller than what MO provides. The small degradation of DOF can be explained by the simplification of SRAF configuration.



(a) Cut line locations for the process window analysis.



(b) Simulated DOF for different OPC techniques.



(c) Exposure latitude vs. depth of focus comparison for different OPC techniques.

Figure 8. Depth of focus and exposure latitude simulation comparison between different OPC techniques.

4. FULL CHIP OPC RESULTS AND DISCUSSION

Full chip OPC was carried out on a test chip of size 22 mm^2. Figure 9 shows the normalized runtime result comparisons. For this particular data, the total runtime using the hybrid OPC with CO-OPT was about 6% longer than what the regular OPC needed. The 6% increase in OPC run time is acceptable for a production tape-out considering the superior correction results with the CO-OPT OPC. However, it is important to note that the correction time needed for CO-OPT OPC directly correlates to the number of hot spot areas or critical areas. A further optimized OPC flow may be needed to address full chip correction with a large number of hot spots.

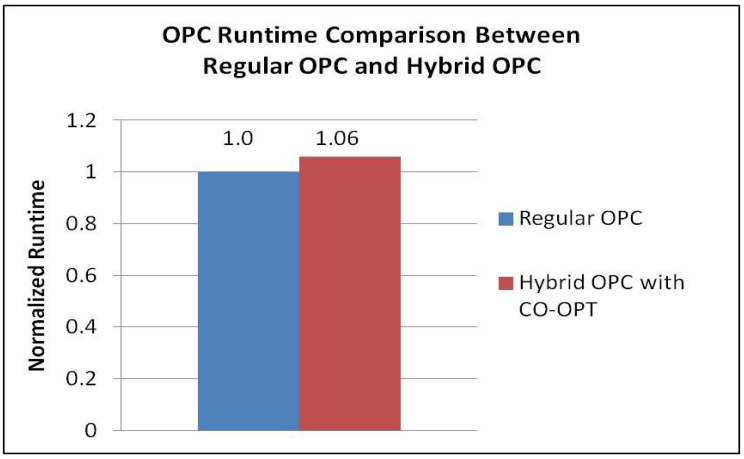


Figure 9. OPC runtime performance for regular OPC and hybrid OPC with CO-OPT OPC.

Full-chip verification also was performed for pinch, bridge, minimum print area, PVBAND and MEEF. Table 2 summarizes the verification results for regular OPC and hybrid OPC with CO-OPT OPC. With CO-OPT OPC, the worst-case bridging is improved from 4 nm below the spec limit to 2 nm above the spec limit, through all PW conditions (focus variation, dose variation and mask bias variation). The minimum printing area through all PW conditions is improved from 100 nm^2 below the spec limit to meeting the spec limit at all process window conditions. The maximum PVBAND is improved by 6 nm to meet the spec limit, and the worst MEEF is improved by 6 to meet the spec limit. The worst pinching errors for all PW conditions are comparable between CO-OPT OPC and regular OPC on the full chip. This can be explained by the fact that the most critical OPC structure is a small space between design targets.

Table 2. Full-chip verification results for pinch, bridge, minimum printing area, PVBAND and MEEF.

	MIN Width at all PW conditions	MIN Space at all PW conditions	MIN Printing Area at all PW conditions	MAX PVBAND	MAX MEEF
Regular OPC	At spec limit	4 nm worse than spec limit	100 nm^2 worse than spec limit	6 nm worse than spec limit	6 worse than spec limit
Hybrid OPC with CO-OPT	At spec limit	2 nm better than spec limit	At spec limit	At spec limit	At spec limit
Improvement	0	6 nm	100 nm^2	6 nm	6

5. CONCLUSIONS

In this paper, we presented a holistic full-chip OPC solution for a 20nm contact layer, through the combination of SMO, SRAF optimization, PWOPC and MF-SRAF CO-OPT OPC. The new SMO illumination source provides improved DOF, EL and MEEF for all the critical patterns. Optimized hybrid SRAF flows provide the needed process window for all the design patterns, while still maintaining process variation consistency for target patterns with similar design. CO-OPT OPC, which optimizes the MFs and SRAFs together with a cost-based multiple variable solver, was applied to selective critical areas after regular OPC was finished. The hybrid OPC flow with CO-OPT OPC improved the DOF, EL

and MEEF significantly for the selected critical areas. A 6% OPC runtime increase was reported on the full-chip correction by using the hybrid OPC flow with CO-OPT OPC.

REFERENCES

[1] DongQing Zhang, et al., "Source mask optimization methodology (SMO) and application to real full chip optical proximity correction," Proc. SPIE 8326, (2012).
[2] Nicolas B. Cobb, Yuri Granik, "Model-based OPC using the MEEF matrix," Proc. SPIE, 4889 (2002).
[3] Yu-Po Tang, et al., "OPC segmentation: dilemma between degree-of-freedom and stability with some relieves," Proc. SPIE, 7274 (2009).
[4] Yang Ping, et al., "Tolerance-based OPC and solution to MRC-constrained OPC," Proc. SPIE, 7973 (2011).